REMARKS

Reconsideration of the instant application is respectfully requested. The present amendment is responsive to the Office Action of June 14, 2005, in which claims 1-18 are presently pending. Of those, claims 1, 2, 6-8, 12-14 and 18 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,604,705 to Ackland, et al. In addition, claims 3, 4, 9, 10, 15 and 16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ackland, in view of U.S. Patent 6,341,083 to Wong. Finally, claims 5, 11 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. For the following reasons, it is respectfully submitted that the application is in condition for allowance.

The present amendment cancels dependent claims 2, 3, 8, 9, 14 and 15 and incorporates the subject matter of the same into their respective independent claims, while dependent claims 4, 10 and 16 are made dependent directly from amended independent claims 1, 7 and 13. Therefore, each of the outstanding §102(b) rejections over Ackland have been rendered moot. With regard to the remaining outstanding §103 rejections of claims 3, 4, 9, 10, 15 and 16 over the combination of Ackland and Wong, the Applicants respectfully traverse the same for the reason that (i) one skilled in the art would not be motivated to combine the teachings of Ackland and Wong for the purpose of arriving at the claimed invention; and (ii) even if so, the combination of the references would not result in effective clamping of the high-side bitline using the Wong SRAM cell.

For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that (1) all elements of the claimed invention are disclosed in the prior art; (2) that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or to combine references; and (3) that

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the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d, 1016, 1023 (Fed. Cir. 1996).

With regard to the second element, there are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998) (The combination of the references taught every element of the claimed invention, however without a motivation to combine, a rejection based on a *prima facie* case of obvious was held improper.). The level of skill in the art cannot be relied upon to provide the suggestion to combine references. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999). Furthermore, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

A statement that modifications of the prior art to meet the claimed invention would have been " 'well within the ordinary skill of the art at the time the claimed invention was made' " because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993). See also *In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1318 (Fed. Cir. 2000).

As acknowledged by the Examiner on page 3 of the Office Action, discrete transistors T14 and T15 of Ackland are used to implement a clamping function that keeps the high-side bitline from falling along with the low-side bitline so that data can be more quickly captured by the sense amplifier. These clamping transistors (as also

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acknowledged by the Examiner) are neither SRAM cell access transistors nor are they part of the SRAM cell itself. In fact, Ackland does not even explicitly show an SRAM cell in the figures thereof; instead, Ackland simply relies on incorporating a conventional cell configuration, such as one disclosed in an earlier patent (5,309,395) referenced by Ackland. By not even depicting an exemplary SRAM cell (or the access transistors thereto) in the specification thereof, Ackland thus teaches away from modifying its sense amplifier to have the high-side bitline clamping function provided by an SRAM cell itself since a conventional SRAM cell uses NFET access devices (which do not pass a logic high voltage).

Moreover, the Examiner has further indicated on page 4 of the Office Action that Wong teaches that the use of SRAM cells with PFET access transistors "improves the cell stability, lowers the cell power dissipation, and requires less surface area." In one respect, the Wong reference, by itself, provides no motivation to use its PFET access transistors or cell pull-up devices as clamps to maintain one of the bitline voltages at a high level, since Wong does not provide any details of the operation of sense amplifier circuitry whatsoever.

Notwithstanding this fact, there is still no teaching in Wong that the PFET access transistors of the SRAM cell can also be used to implement a clamping function for maintaining any signal (much less a high-side bitline) to thereby improve the signal development time when reading data from the SRAM cell. On the contrary, since a primary purpose of Wong is to reduce cell area by using smaller PFET devices with respect to conventional NFET devices (Wong, col. 3, lines 50-65), it stands to reason that the internal PFET pull-up devices of the Wong SRAM cell would not be capable of sufficiently clamping a high-side bitline voltage to the logic high value, in the manner presently claimed. This is even further evidenced by previously allowable claims 5, 11, and 17, in which it is further claimed that the PFET devices of the cell have larger pull-up strengths than the counterpart pull-down strengths of the corresponding NFET devices of the cell.

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Accordingly, one skilled in the art would not be motivated to implement the (discrete device) high-side bitline clamping function of Ackland with the PFET access transistors of Wong to arrive at the presently claimed invention. Since Wong strives for cell size reduction, this reference actually teaches away from using the cell access transistor (and hence the using the cell's pull-up transistors as clamping devices) since such an application would necessarily limit the extent to which the pull-up devices can be minimized while also providing sufficient clamping strength. Thus, even if one skilled in the art were to modify the teachings of Ackland to provide high-side bitline clamping through a PFET access SRAM cell as taught by Wong, the resulting combination thereof would not provide effective high-side bitline clamping due to the limited strength of the small devices in Wong.

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Therefore, for the reasons outline above, the Applicants respectfully submit that the outstanding rejections §103 over the combination of Ackland and Wong have been overcome and that the present amendment places the application in condition for allowance. No new matter has been entered and no additional fees are believed to be required. However, if any fees are due with respect to this Amendment, please charge them to Deposit Account No. 06-1130 maintained by Applicants' attorneys.

Respectfully submitted,
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